Real-Time Classification of Myocardial Ischemia for Portable Embedded Systems

Post-Doctoral Offer – 15 months

Keywords
Biomedical electronics, Edge AI, Embedded systems, Machine Learning, myocardial ischemia, FPGAs, ASICs

Background and objectives

The GeePs laboratory is recruiting a post-doctoral researcher to participate in an ambitious project to develop a portable embedded system capable of detecting, in real time, episodes of myocardial ischemia in patients at risk.

This project builds on previous work [1] that led to the design of ECG acquisition and real-time digital pre-processing electronics, optimized for noise filtering while preserving the integrity of the ST segment, the main indicator of myocardial ischemia.

The objective of the post-doctoral fellowship is to design, implement and validate a frugal classification algorithm, adapted to a future ASIC integration (XH018 technology), with a functional demonstrator on FPGA as the main deliverable.

Bibliography

[1] Guénégo, B. (2023) *Conversion numérique de signaux biologiques de faibles intensités pour les applications biomédicales*. PhD thesis, Université Paris-Saclay. Available on http://www.theses.fr/2023UPAST230.

Provisional progress of the post-doc

Phase 1 – Analysis and Algorithmic Design (Months 1-6)

- State of the art on the detection of myocardial ischemia from ECG signals and the embedded analysis of these signals.
- Feature selection: determination of the most relevant features to be extracted from the wavelet decomposition of the ECG for robust ischemia detection.
- Identification algorithm: development of methods for the efficient estimation of the selected features.
- Classifier development: design for a frugal implementation on an embedded system compatible with the constraints of the application.

Phase 2 – Hardware implementation and demonstrator (months 7 to 15)

- VHDL implementation: FPGA architecture, synthesis, and layout.
- Demonstrator design: integration of hardware components (FPGA board, ADC, analog front-end) to validate the system.

- Tests: Evaluation of functional and temporal performance on realistic signals.
- *(Depending on the state of progress)* ASIC integration preliminary study (XH018): synthesis, layout, estimation of surface area and consumption.

Valuation and prospects

The above work is intended to be presented at conferences and to be the subject of scientific articles in peer-reviewed journals.

Desired profile

- PhD in Digital Electronics, Signal Processing, or related discipline
- Strong skills in real-time embedded systems
- Experience in development and optimized implementation of algorithms for constrained systems (power, surface)
- Proficiency in Python and/or Matlab
- Proficiency in VHDL and FPGA tools (synthesis, layout)
- Initiative, scientific rigor and teamwork skills
- Good command of English (written and oral)

Contacts

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- Morgan Roger at morgan.roger@centralesupelec.fr or +33 1 75 31 78 91

To apply, please send your résumé, a cover letter, as well as the contact details of two references to caroline.lelandais-perrault@centralesupelec.fr & morgan.roger@centralesupelec.fr before 16/06/2025.

Location: GeePs Laboratory – CentraleSupélec – Université Paris-Saclay, 11 rue Joliot Curie 91192 Gif-sur-Yvette

Dates: 15 months from October 2025